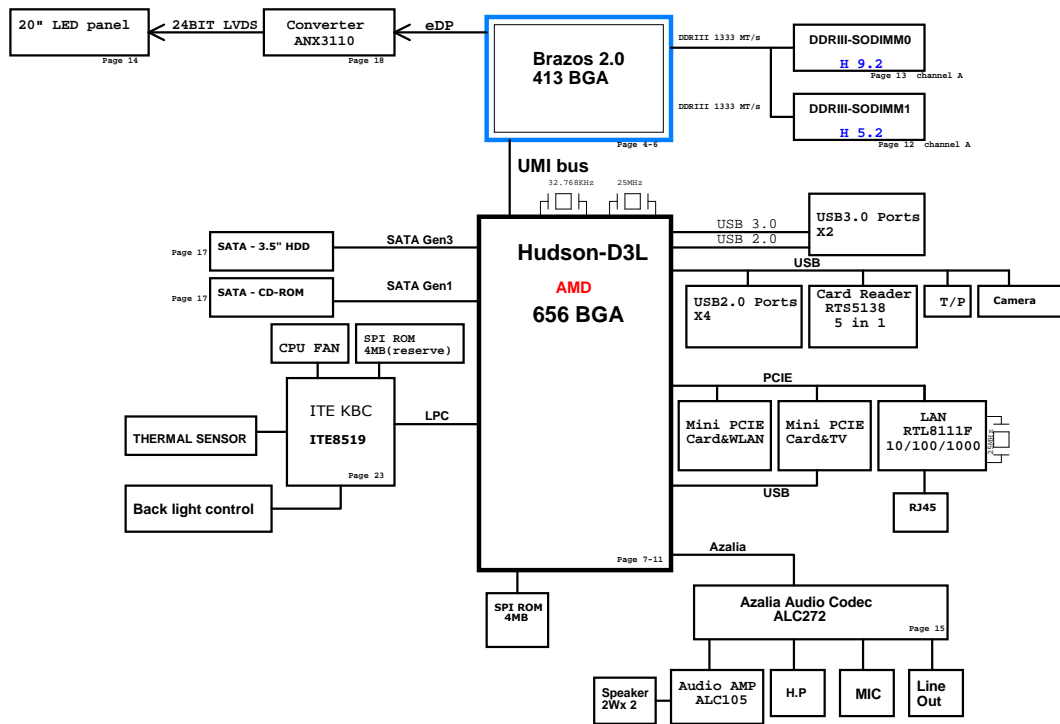


QK3B UMA BLOCK DIAGRAM



PCB STACK UP

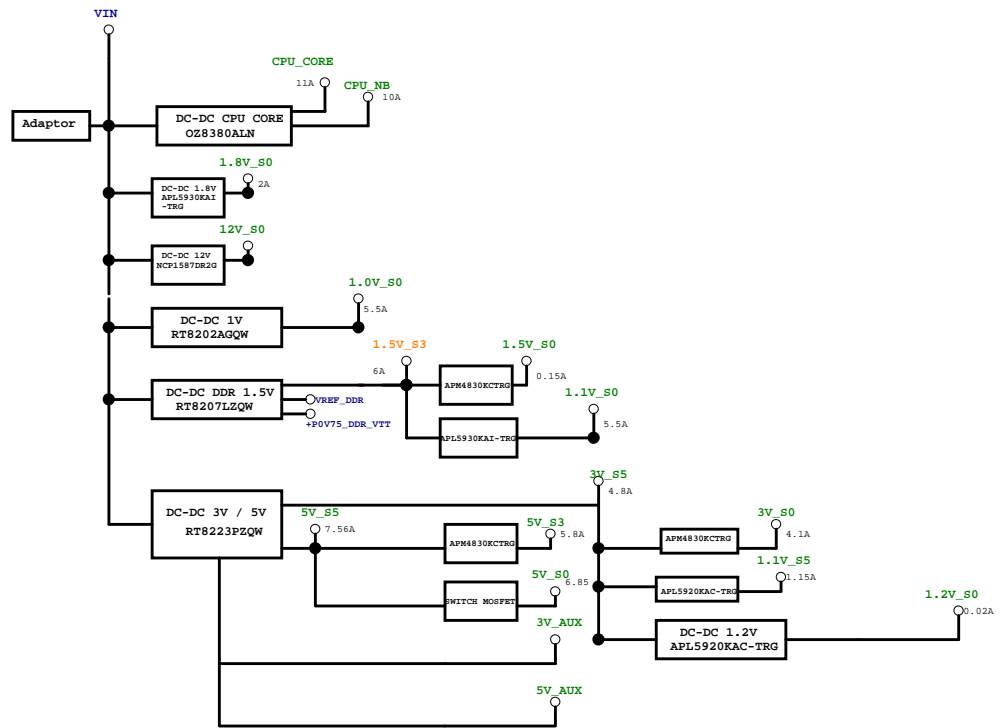
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : Bottom

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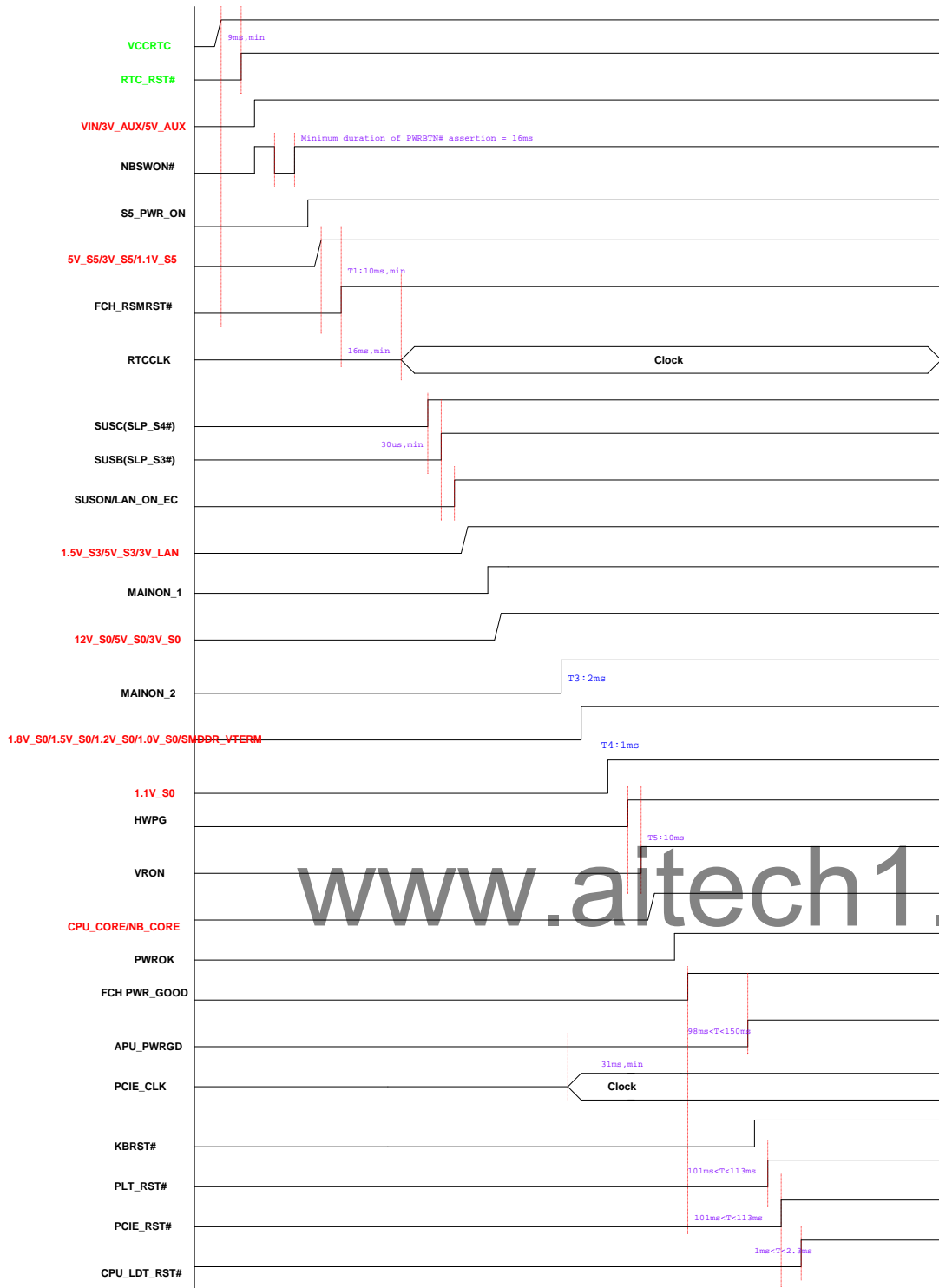
Voltage Rails

Power	Voltage	S0	S3	S4	S5	G3	Ctl Signal
VCCRTC	3V	ON	ON	ON	ON	ON	
VIN	19.5V	ON	ON	ON	ON	OFF	Adaptor IN
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor IN
3V_AUX	3.3V	ON	ON	ON	ON	OFF	Adaptor IN
5V_S5	5V	ON	ON	ON	ON	OFF	5V_PWR_ON
3V_S5	3.3V	ON	ON	ON	ON	OFF	3V_PWR_ON
1.1V_S5	1.1V	ON	ON	ON	ON	OFF	5V_PWR_ON
5V_S3	5V	ON	ON	OFF	OFF	OFF	BURON
1.5V_S3	1.5V	ON	ON	OFF	OFF	OFF	BURON
3V_LAN	3V	ON	Note	Note	Note	OFF	LAN_ON_EC
12V_S0	12V	ON	OFF	OFF	OFF	OFF	MANON_1
5V_S0	5V	ON	OFF	OFF	OFF	OFF	MANON_10
3V_S0	3V	ON	OFF	OFF	OFF	OFF	MANON_10
1.8V_S0	1.8V	ON	OFF	OFF	OFF	OFF	MANON_1
1.5V_S0	1.5V	ON	OFF	OFF	OFF	OFF	MANON_10
1.2V_S0	1.2V	ON	OFF	OFF	OFF	OFF	MANON_1
1.1V_S0	1.1V	ON	OFF	OFF	OFF	OFF	MANON_1
1.0V_S0	1.0V	ON	OFF	OFF	OFF	OFF	MANON_1
SMOOR_VTERM	6.75V	ON	OFF	OFF	OFF	OFF	MANON_1
CPU_CORE	By VID	ON	OFF	OFF	OFF	OFF	VRON
MB_CORE	By VID	ON	OFF	OFF	OFF	OFF	VRON

Note: Depend on WOL



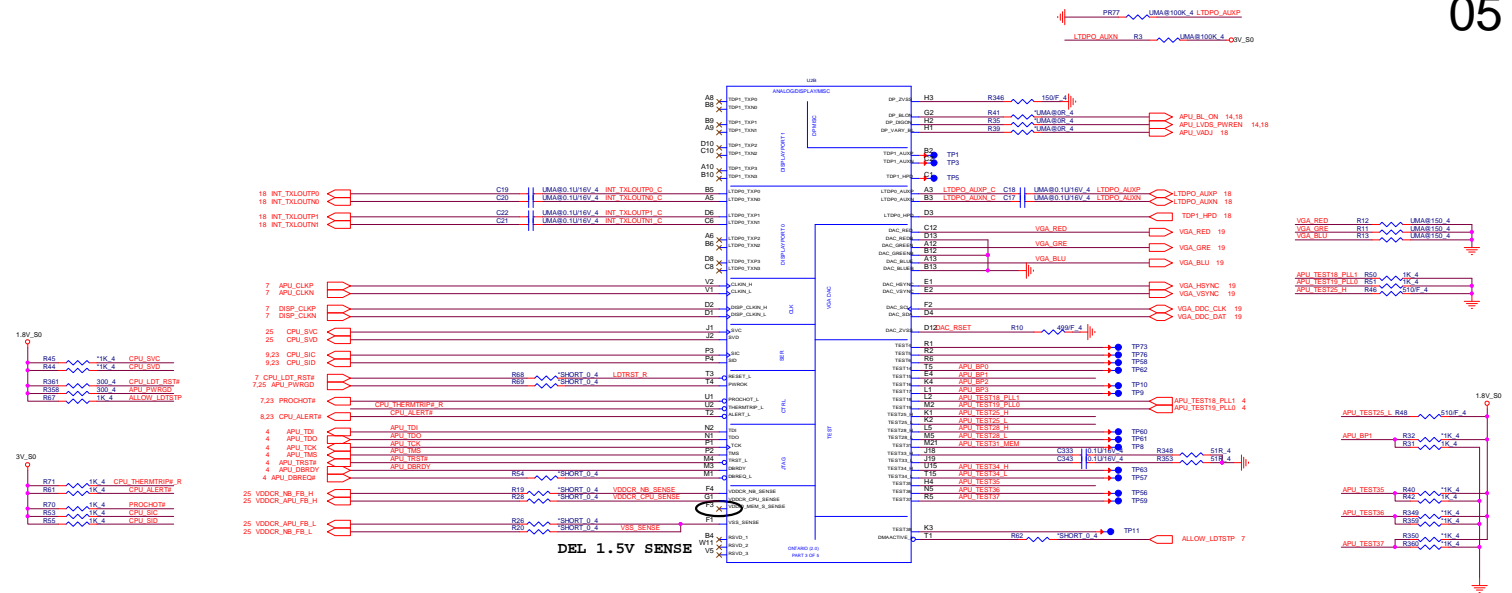
QK3B Power On/Off Sequencing Timing Diagram

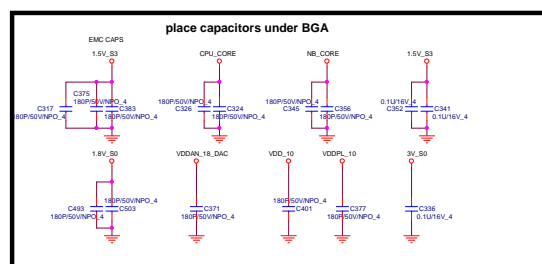
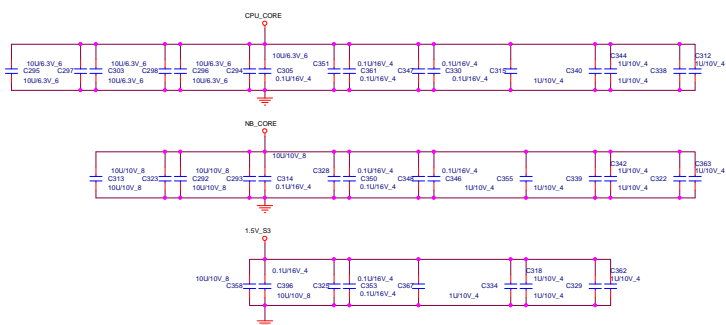
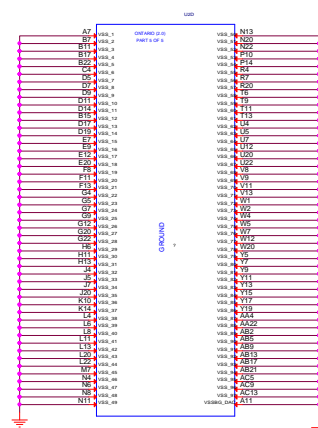
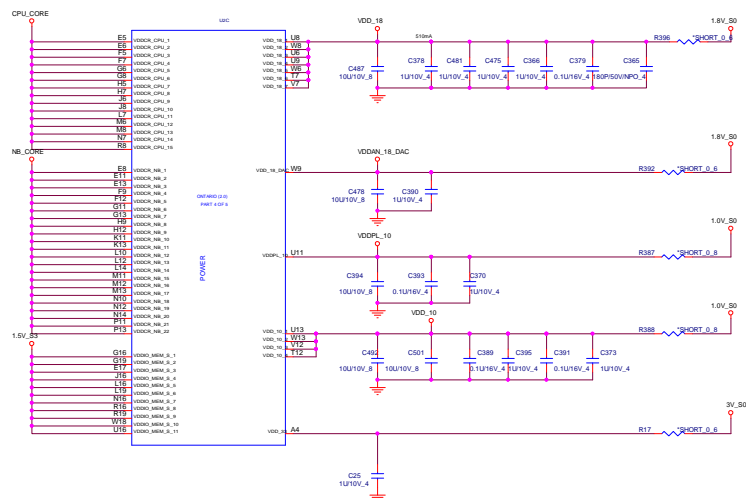


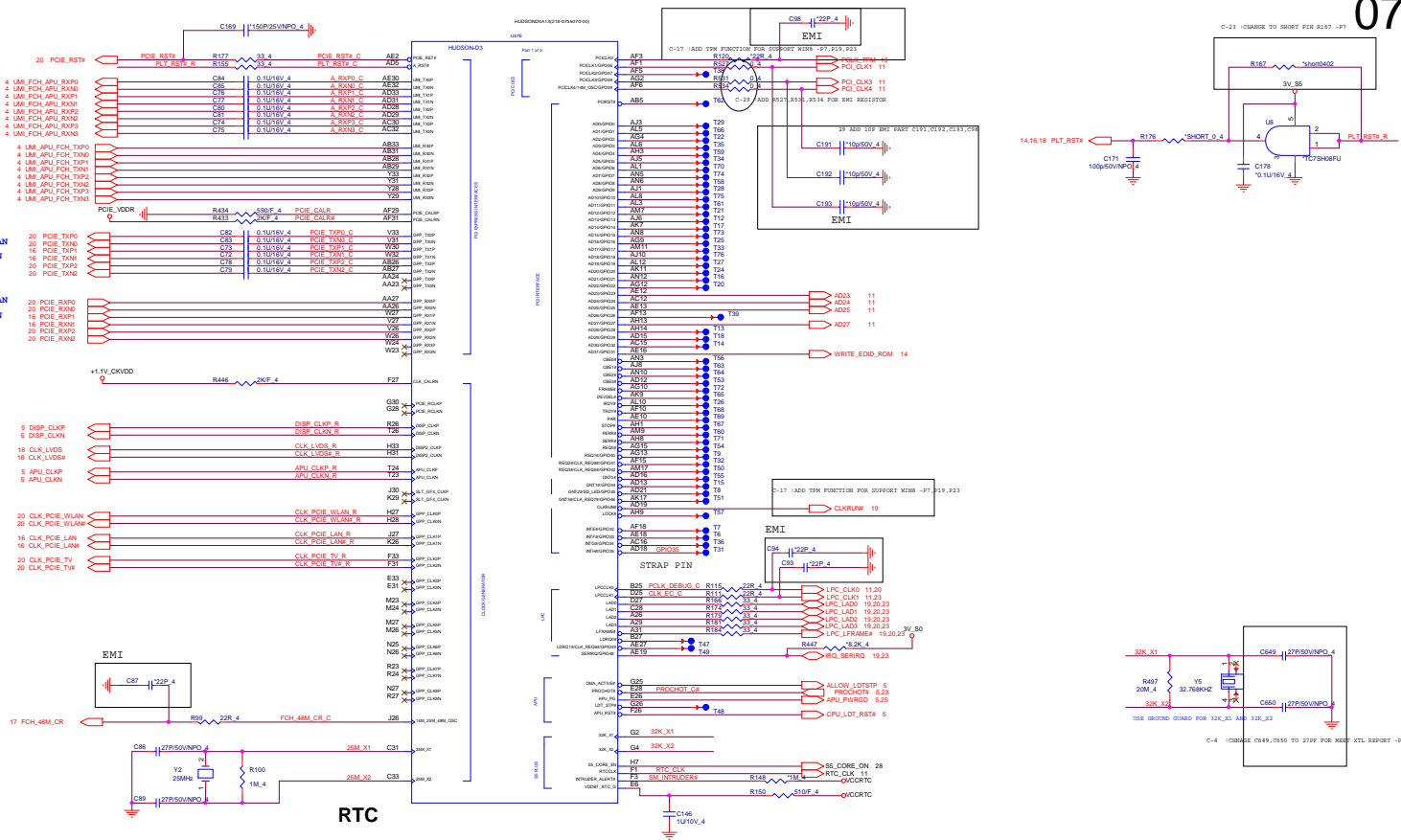
EC CONTROL SIGNAL

SPNO	MIN	MAX	Control signal	Time
T1	10ms		S5_PWR_ON->FCH_RSMRST#	15ms
T4			MAIN_ON2->MAINON_3	1ms
T5			HWPG->VRON	10ms

NOTE:
1.VV_S5=1.1V_S5(for system)
2.VOC3=VOC1.8>VOC1.1(for system)
3.VOC3=VOC1.2(For DP to LVDS converter)
4.VOC3=VOC1.5(For TV Card)



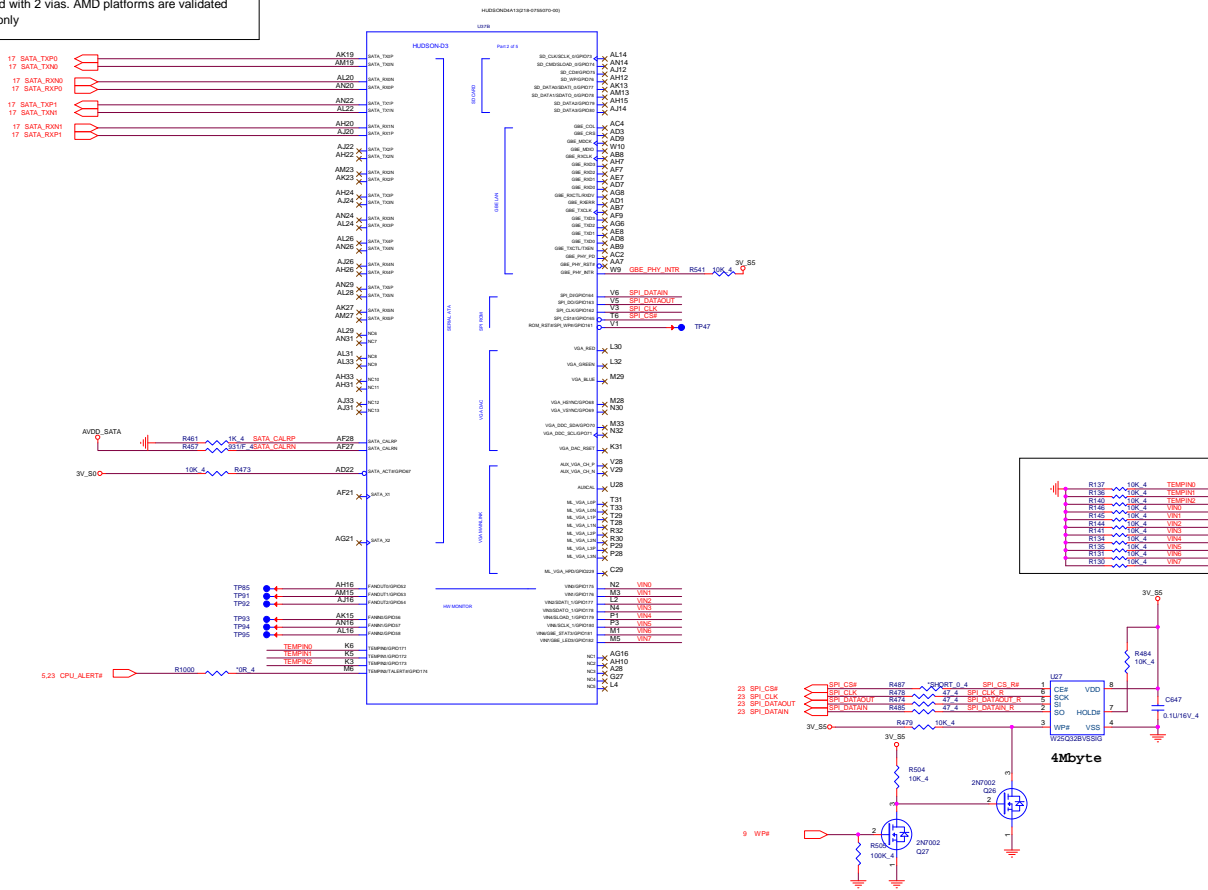




SATA trace should use only 1via on the trace.
customers can use 2vias with GND via within 150mils of signal via as long as they can ensure that their platform meets SATA logo requirements. Return loss is expected to get affected with 2 vias. AMD platforms are validated with one via only

ODD

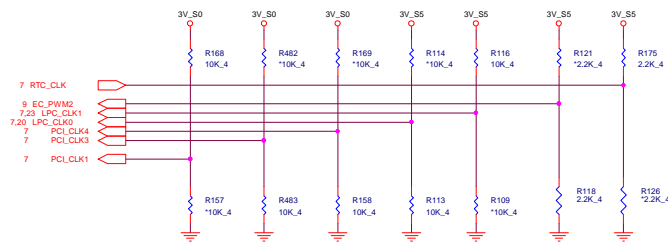
HDD



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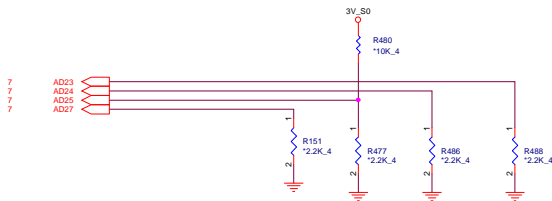


REQUIRED STRAPS



	LPC_CLK0	EC_PWM2	RTC_CLK	LPC_CLK1	PCI_CLK1	PCI_CLK3	PCI_CLK4
PULL HIGH	EC ENABLED	LPC ROM	Set S5 Plus Mode Disable V	Integrated clock mode: Use 25MHz crystal clock and generate both internal and external clocks. V	PCIe interface is at Gen II mode. V	Select external Debug Straps	Reserved
PULL LOW	EC DISABLED V	SPI ROM V	Set S5 Plus Mode Enable	External clock mode: Use 100 Mhz PCIe clock as reference clock and generate internal clocks only.	Force PCIe interface at Gen I mode.	Disable Debug Straps V	Required setting for integrated clock mode V

DEBUG STRAPS



	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	Use internal PLL-generated PLL CLK. V	Normal REFCLK V	Default PCIe straps V	Use ROMTYPE straps to determine the ROM type. V
PULL LOW	Bypass internal PLL clock.	Inverted REFCLK	EEPROM PCIe straps	Route ROM fetch to PCI bus on the very first boot. Use ROMTYPE to determine the ROM type on subsequent boots.



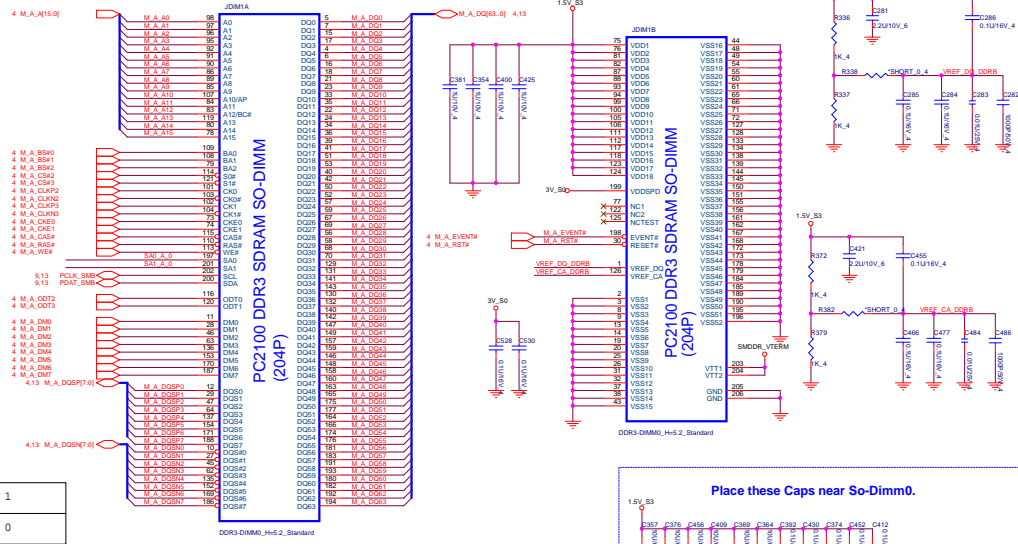
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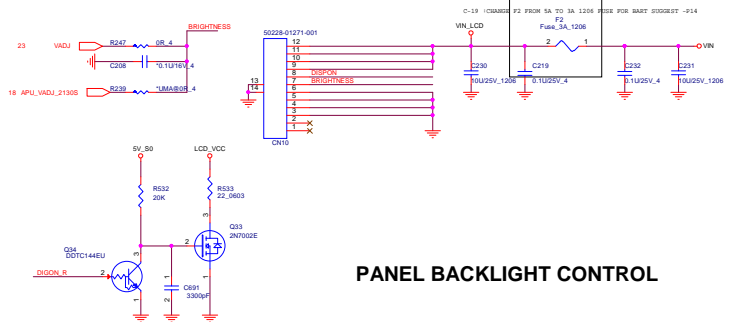
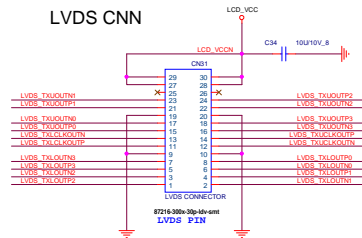
CHANNEL A DIMM 1 H5.2



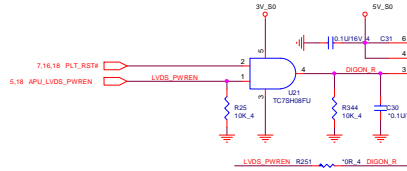
PWM CONTROL

CONVERTER CON

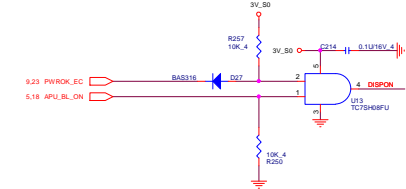
LVDS CNN



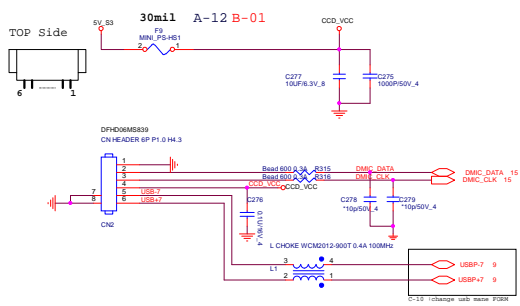
PANEL VCC CONTROL



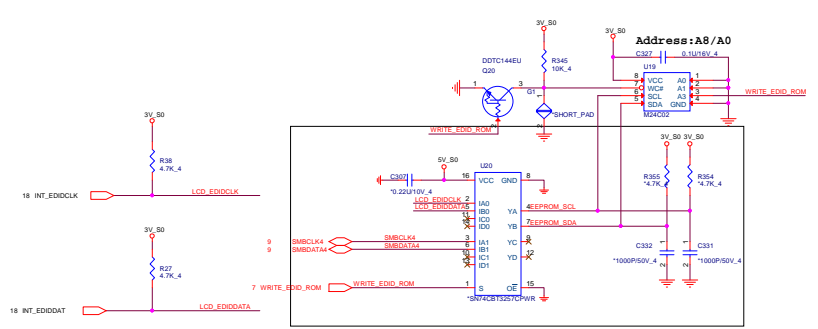
PANEL BACKLIGHT CONTROL



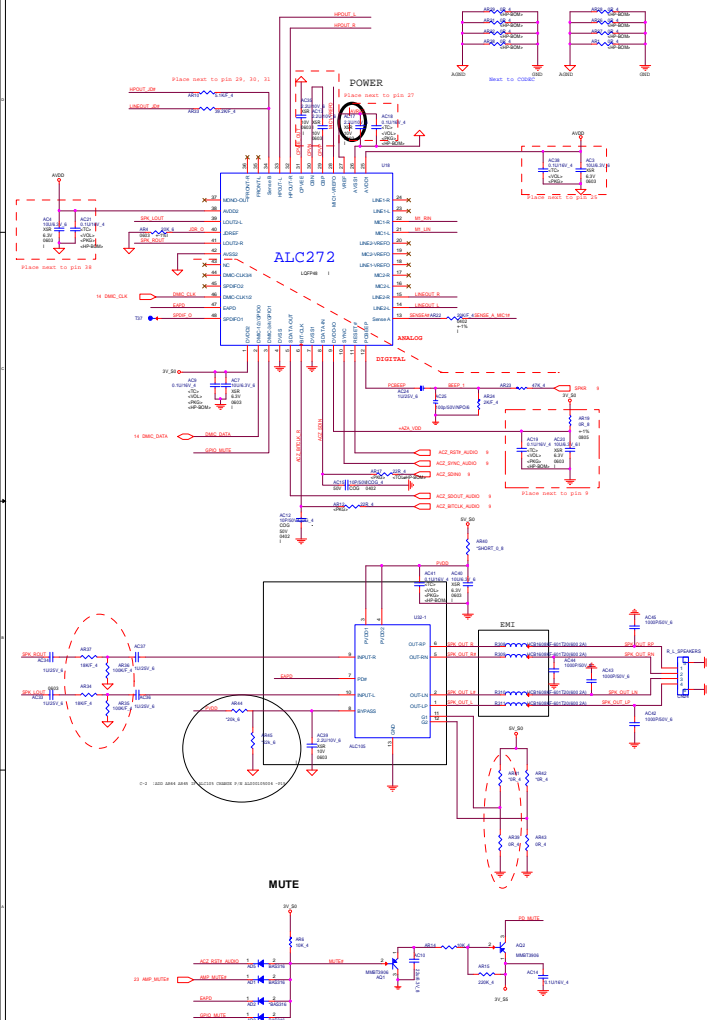
WEB CAM



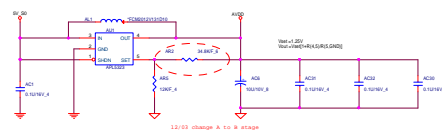
EEPROM IIC Selection



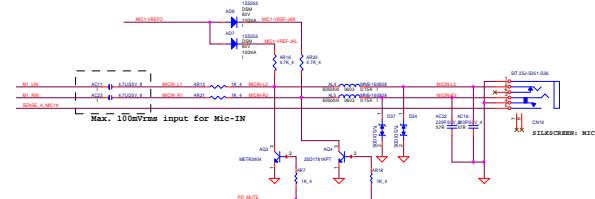
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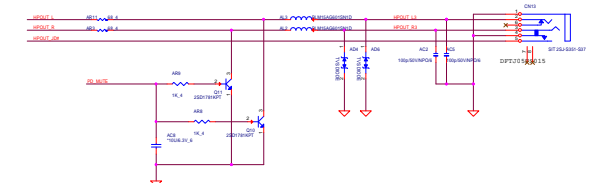
LDO



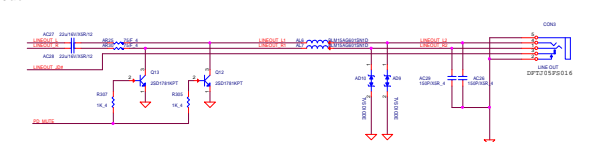
SYSTEM MIC



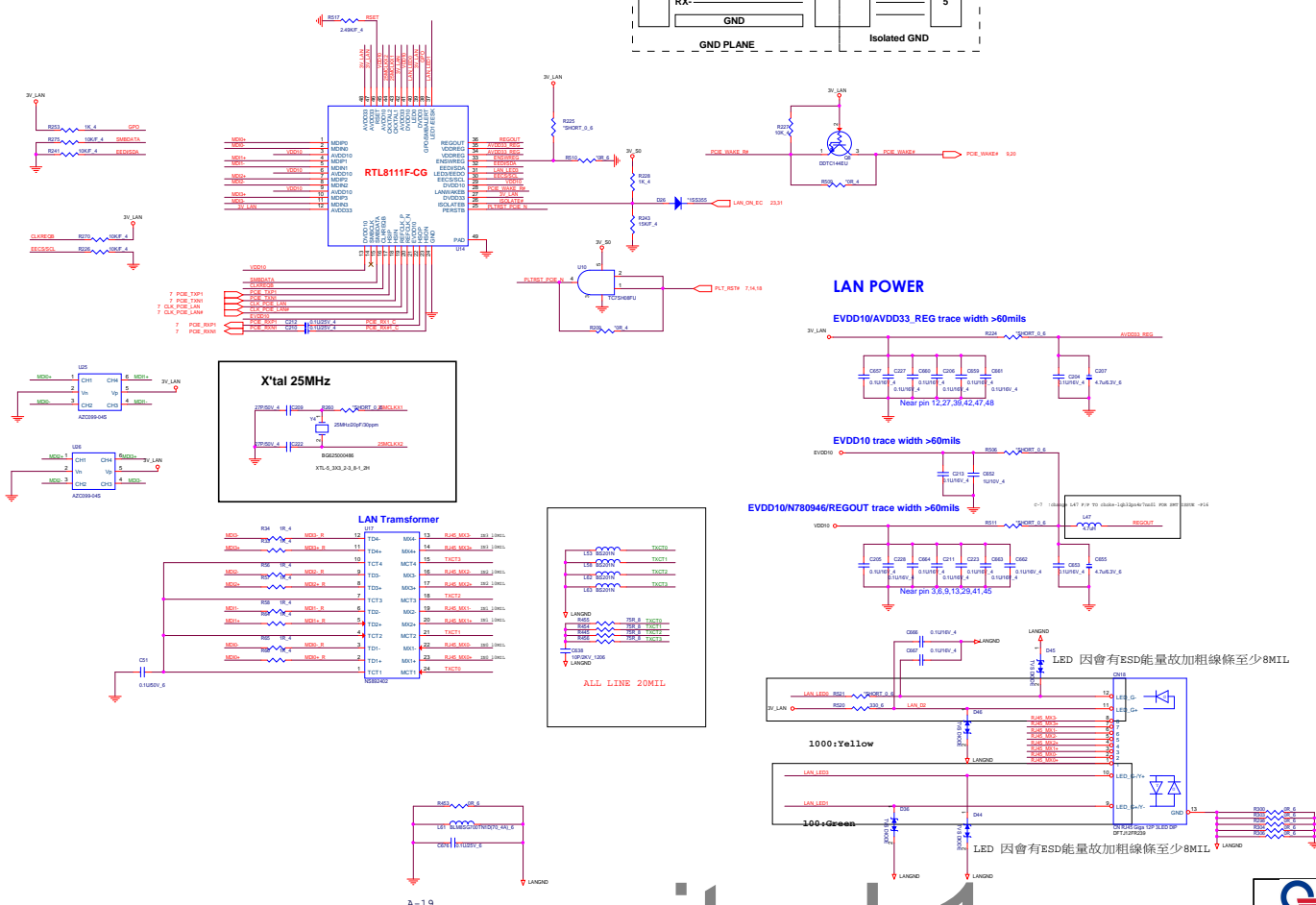
Head Phone



Line Out

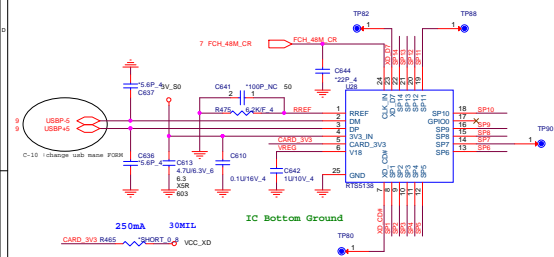


RTL8111F



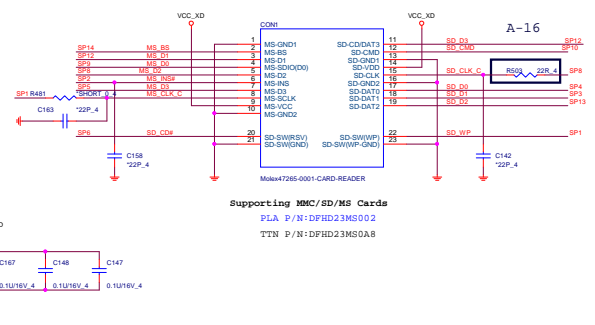
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Card reader RTS5138

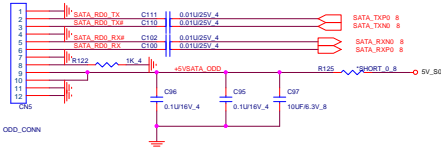


SP1	SD_WP	MS_CLK
SP2		MS_INSP
SP3	SD_D1	
SP4	SD_D0	
SP5		MS_D3
SP6	SD_CD#	
SP8	SD_CLK	MS_D2
SP9		MS_D0
SP10	SD_CMD	
SP12	SD_D3	MS_D1
SP13	SD_A0	
SP14		MS_B3

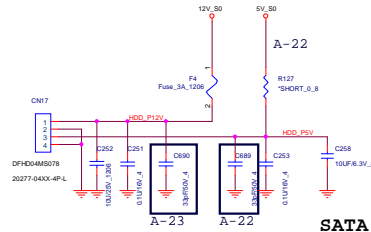
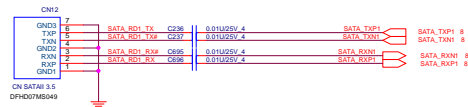
Share Pin



SATA ODD



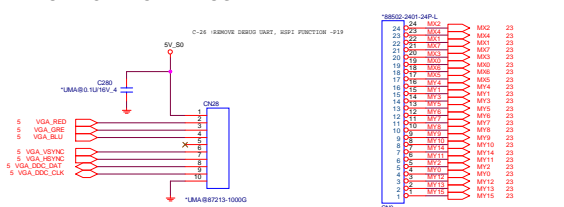
SATA HDD(3.5")



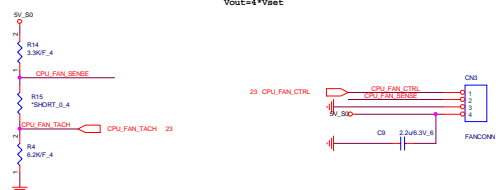
SATA Re-driver IC

UMA CRT FOR DEBUG

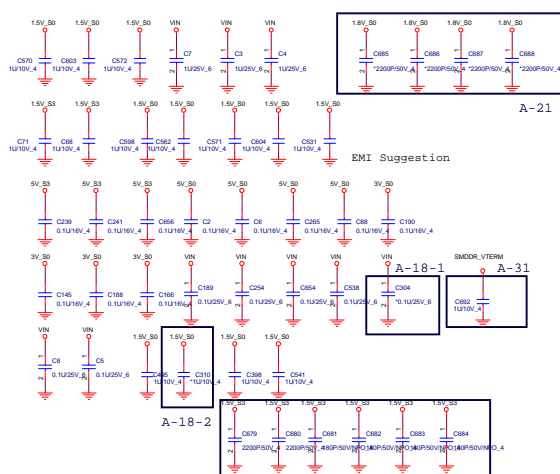
HSPI Debuh Port



System FAN CONN

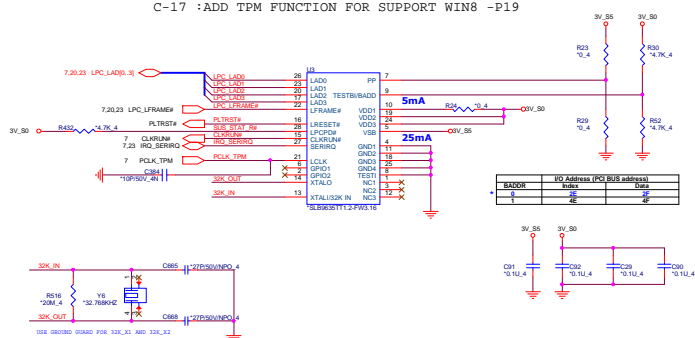
$$V_{out} = 4 \cdot V_{set}$$


Decoupling Cap

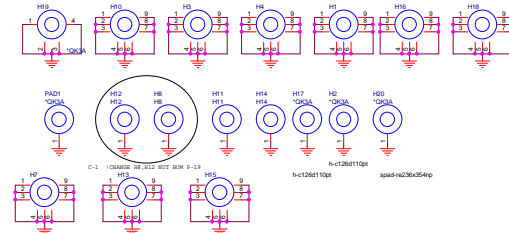


TPM

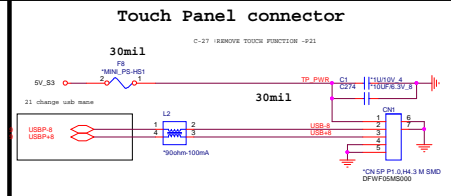
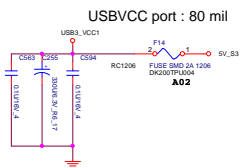
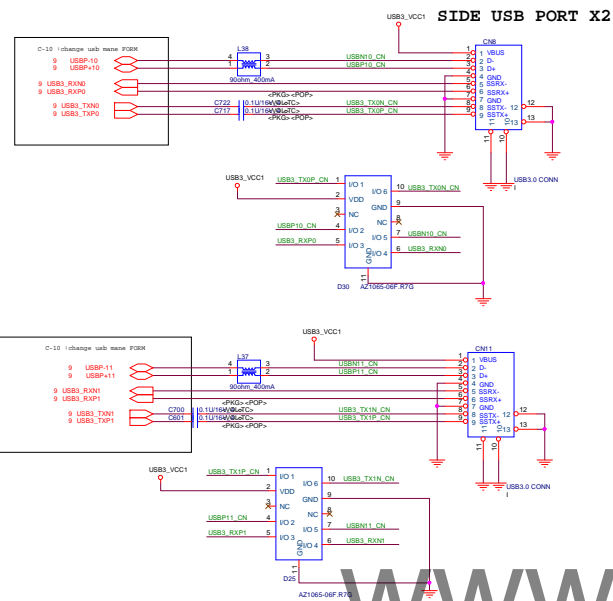
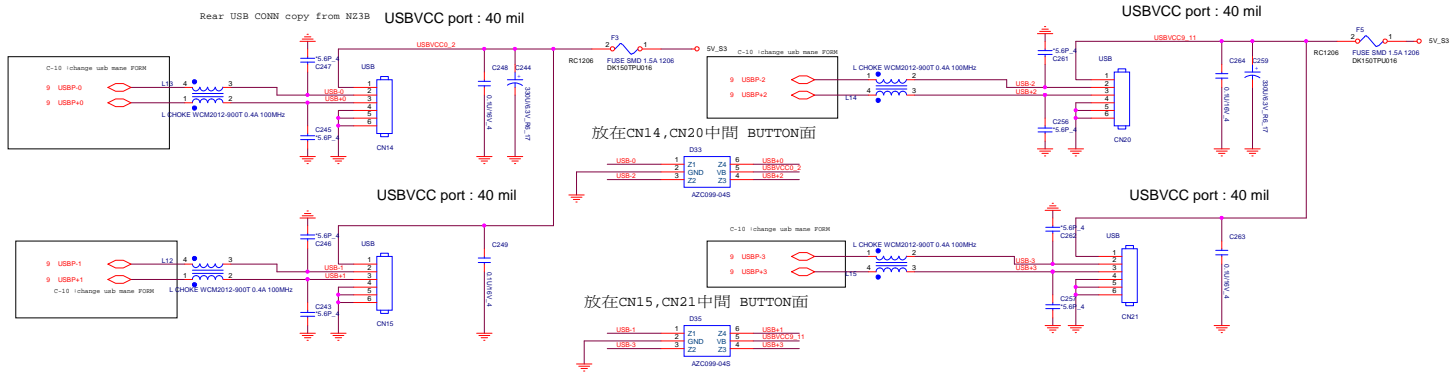
C-17 :ADD TPM FUNCTION FOR SUPPORT WIN8 -P19



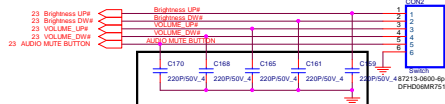
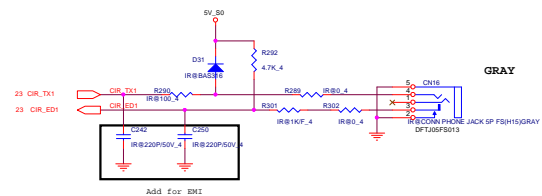
CPU BLK



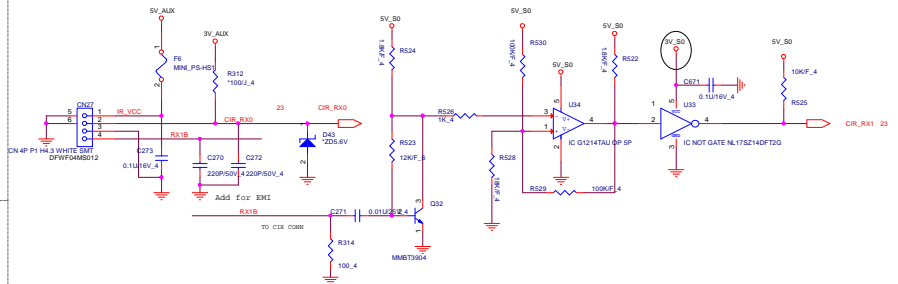
REAR USB PORT X4



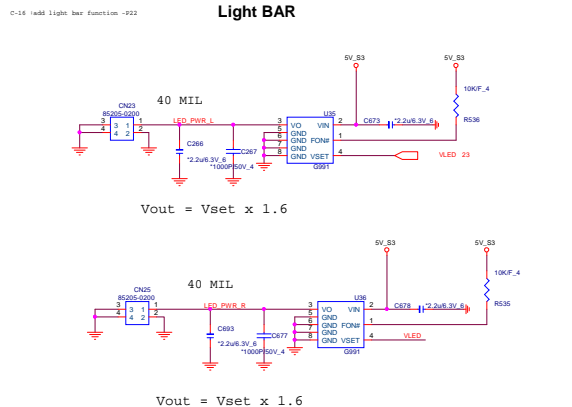
C-28 (REMOVE DEBUG FUNCTION SW1.D42.LED2.LED3) -P22

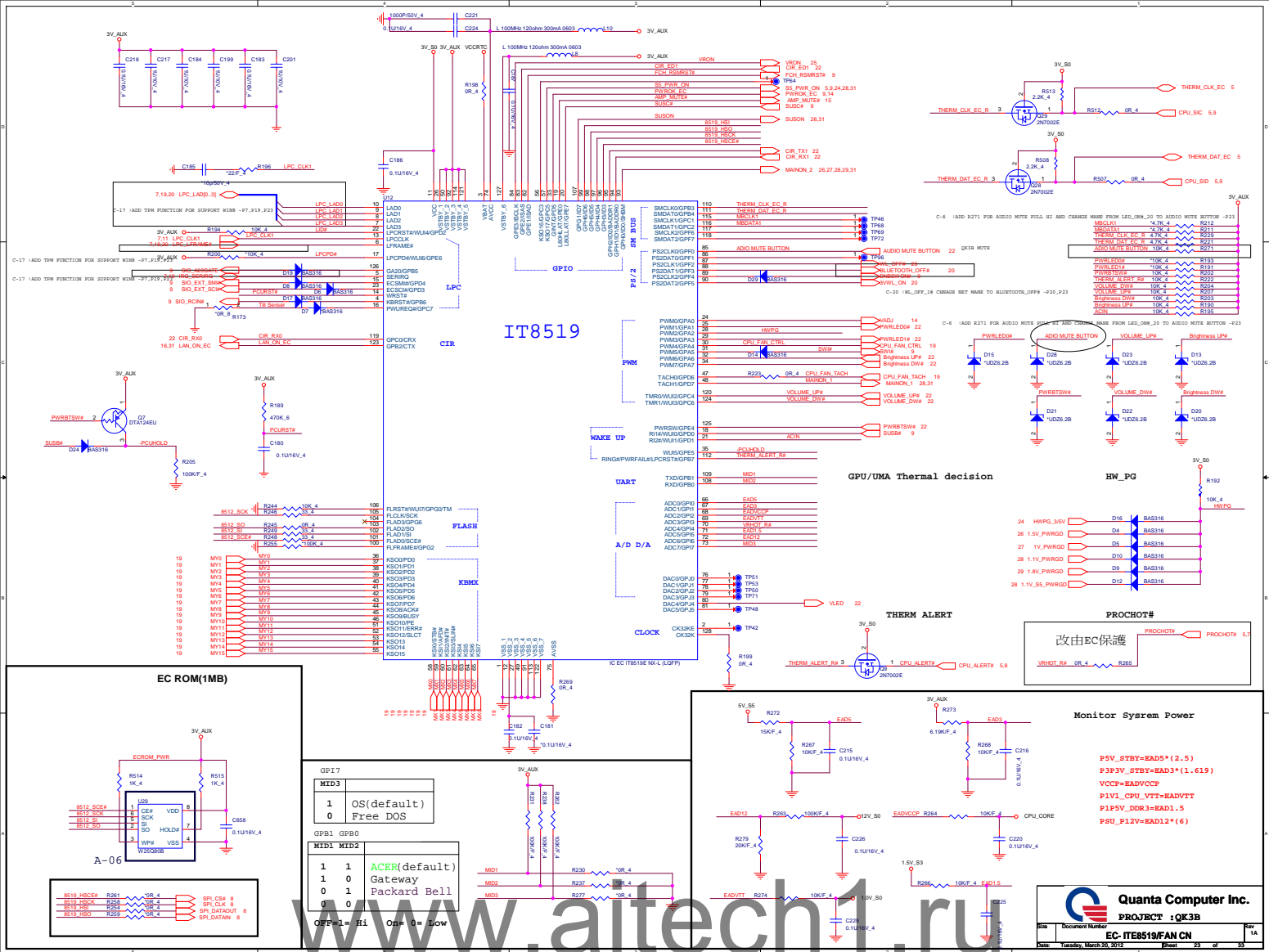


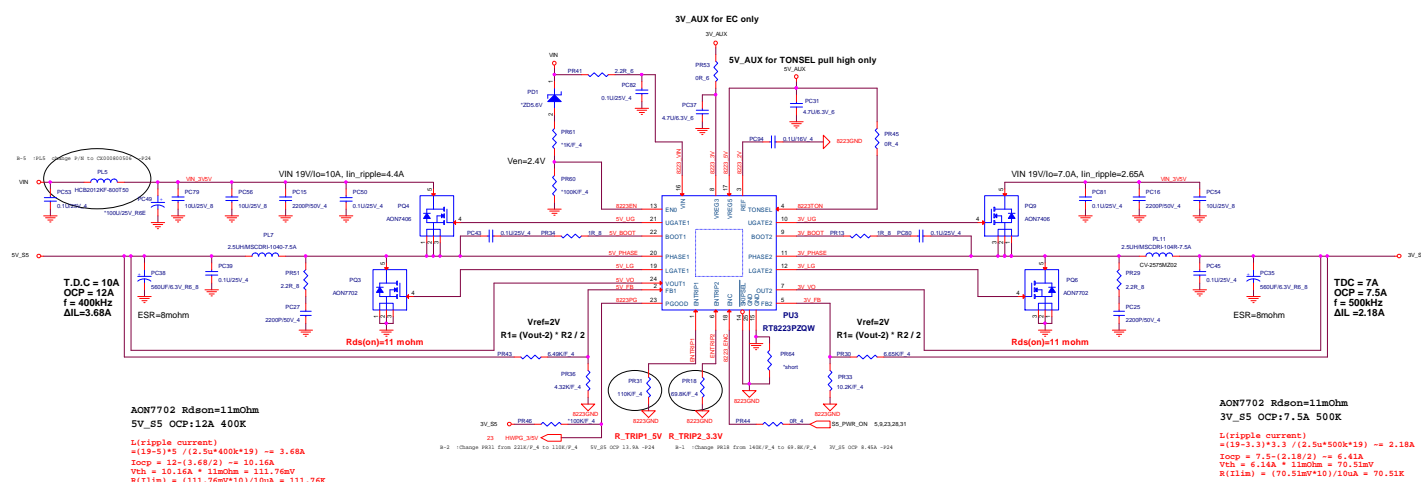
IR Receiver



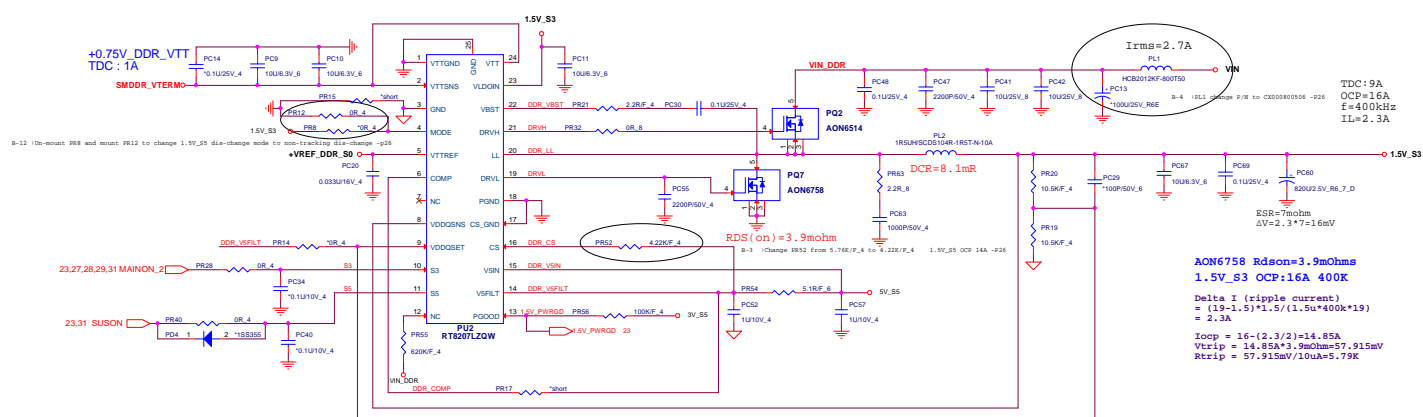
Light BAR



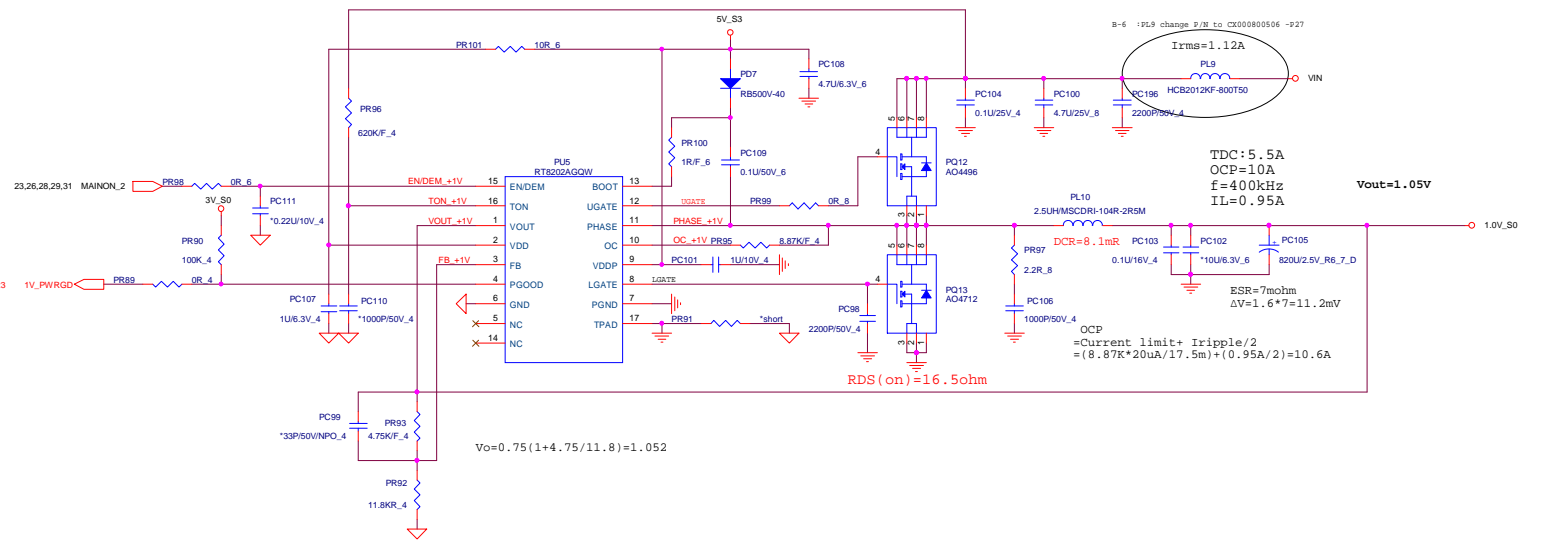





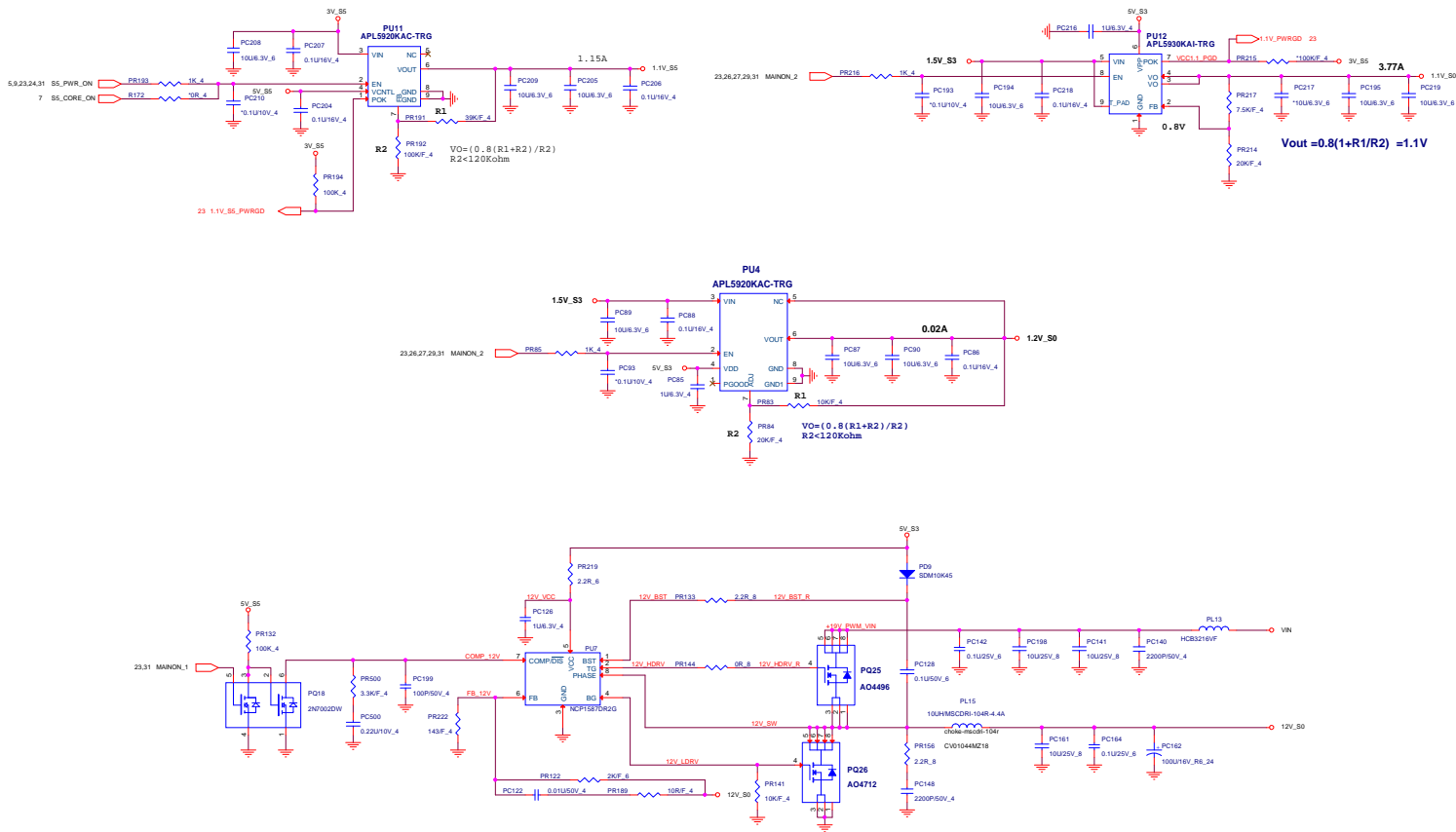




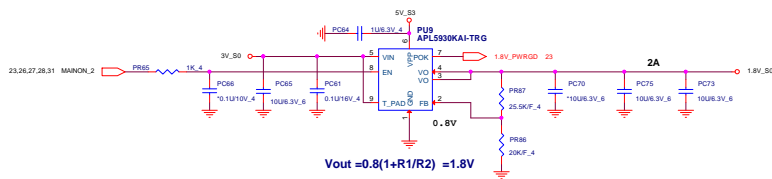
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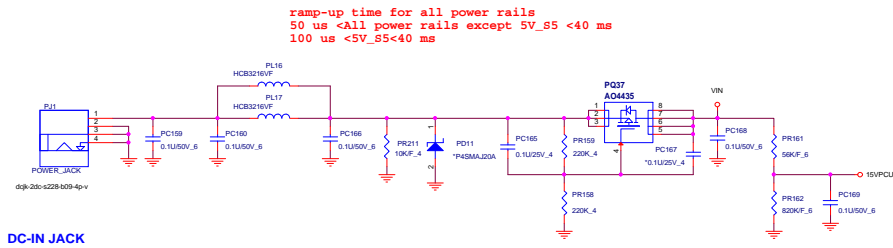
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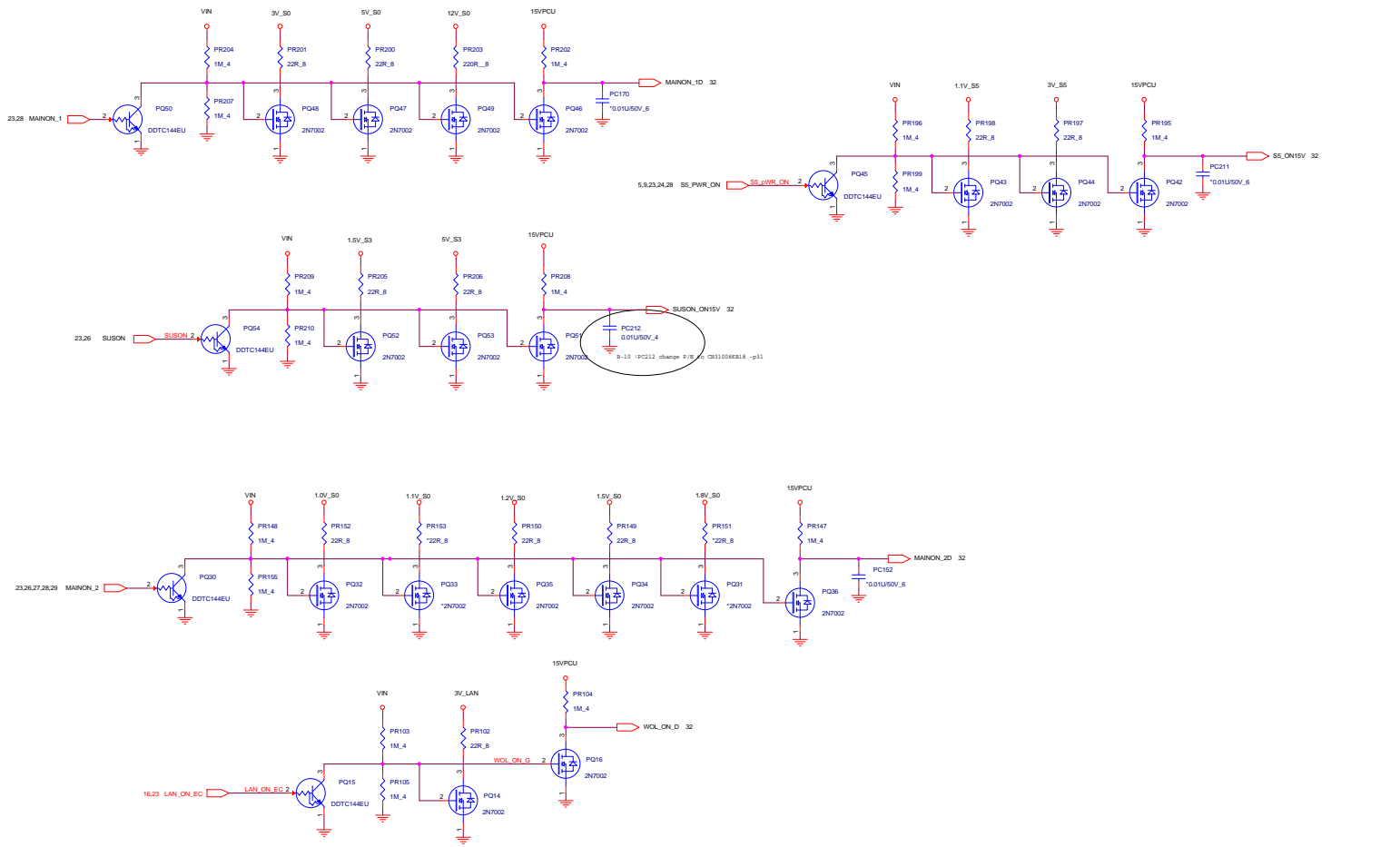


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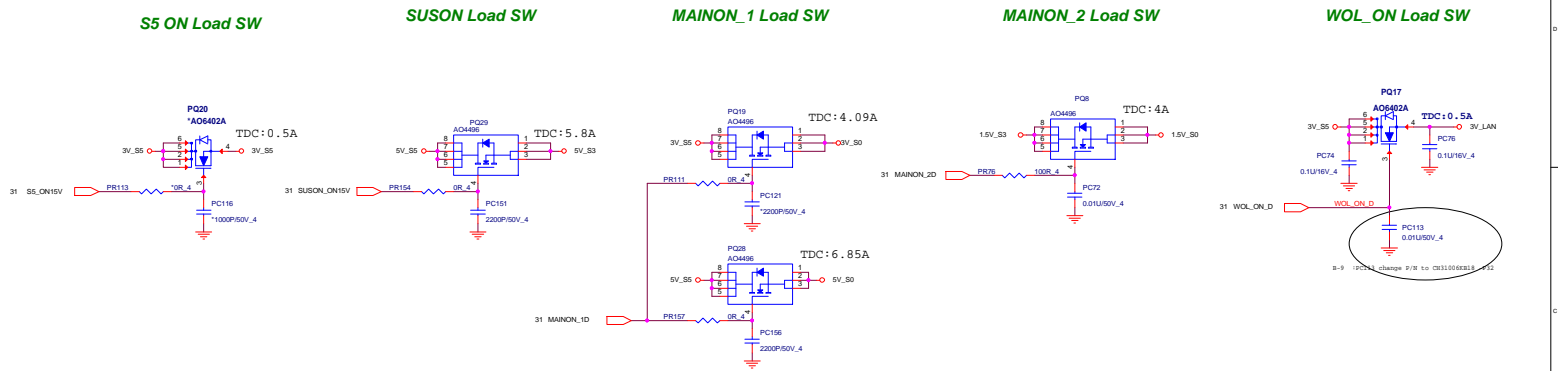


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LOAD SWITCH

	5		3		2		1	
	STAGE		ITEM					
D	QK3B A-B STAGE 2012.1.12		B-1 :Change PR18 from 140K/F_4 to 69.8K/F_4 3V_S5 OCP 8.45A -P24 B-2 :Change PR31 from 221K/F_4 to 110K/F_4 5V_S5 OCP 13.9A -P24 B-3 :Change PR52 from 5.76K/F_4 to 4.22K/F_4 1.5V_S5 OCP 14A -P26 B-4 :PL1 change P/N to CX000800506 -P26 B-5 :PL5 change P/N to CX000800506 -P24 B-6 :PL9 change P/N to CX000800506 -P27 B-7 :PC51 change P/N to CH31006KB18 -P25 B-8 :PC58 change P/N to CH31006KB18 -P25 B-9 :PC113 change P/N to CH31006KB18 -P32 B-10 :PC212 change P/N to CH31006KB18 -p31 B-11 :PC133, PC176 change P/N to CH21006JB10 -p25 B-12 :Un-mount PR8 and mount PR12 to change 1.5V_S5 dis-change mode to non-tracking dis-change -p26 B-13 :Remove PR71 to adjust OZ8380A switching frequency -p25 B-14 :Change PR26 from 19.6K/F_4 to 10K/F_4 CPU_Core & NB_Core OCP 22.5A -p25					D
C	QK3B B-C STAGE 2012.2.13		C-1 :CHANGE H8,H12 NUT BOM P-19 C-2 :ADD AR44 AR45 IF ALC105 CHANGE P/N AL000105004 -P15 C-3 :ADD Q44 FOR WIRELESS WEAK UP AN REMOVE R165 -P20 C-4 :CHNAGE C649,C650 TO 27PF FOR MEET XTL REPORT -P7 C-6 :ADD R271 FOR AUDIO MUTE PULL HI AND CHANGE MANE FROM LED_ON#_20 TO AUDIO MUTE BUTTON -P23 C-7 :change L47 F/P TO choke-lqh32pn4r7nn01 FOR SMT ISSUE -P16 C-8 :ADD SCALAR TEST PAD T40,T5 -P18 C-9 :for wireless weak up change FROM 3V_S0 to 3VWL POWER -P20 C-10 :change usb mane FORM USB 13 CHANGE TO USB 8 -P9,P21 USB 3 CHANGE TO USB 7 -P9,P14 USB 12 CHANGE TO USB 5 -P9,P17 USB 9 CHANGE TO USB 3 -P9,P21 USB 4 CHANGE TO USB 2 -P9,P21 C-11 :Remove short Resistor PR88 for 5V_S5 -P24 C-12 :Remove short Resistor PR94 for 3V_S5 -P24 C-13 :Remove short Resistor PR82 for 1.5V_S5 -P26 C-14 :Remove short Resistor PR81 for 1.0V_S0 -P27 C-15 :Remove short Resistor PR80 for 12V_S0 -P28 C-16 :add light bar function -P22 C-17 :ADD TPM FUNCTION FOR SUPPORT WIN8 -P7,P19,P23 C-18 :ADD 10P EMI PART C191,C192,C193,C98 -P7 C-19 :CHANGE F2 FROM 5A TO 3A 1206 FUSE FOR BART SUGGEST -P14 C-20 :WL_OFF_1# CHNAGE NET MANE TO BLUETOOTH_OFF# -P20,P23 C-22 :REMOVE DEBUG FUNCTION HDT CONNECT -P4 C-23 :CHANGE TO SHORT PIN R167 -P7 C-24 :REMOVE DEBUG FUNCTION FOR EC UPDATA FUNCTION AND ADD R75,R76 -P14 C-25 :CHANGE TO SHORT PIN R6,R7,R8,R36,R37 -P18 C-26 :REMOVE DEBUG UART, HSPI FUNCTION -P19 C-27 :REMOVE TOUCH FUNCTION -P21 C-28 :REMOVE DEBUG FUNCTION SW1,D42,LED2,LED3 -P22 C-29 :ADD R527,R531,R534 FOR EMI RESISTOR -P7 C-30 :CHANGE TO SHORT PIN R183 -P20					C
B								B
A								A
			<div><div>Title</div><div><Title></div><div>Size A</div><div>Document Number</div><div>Rev <RevCo</div><div>Date: Tuesday, March 20, 2012</div><div>Sheet 33 of 33</div></div>					
	5		4		3		2	